REMARKS

Claims 1-15 are pending in this application. By this Amendment, claims 1 and 6 are amended and new claims 10-15 are added. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made."

The Office Action rejects claims 1-9 under 35 U.S.C. § 112, second paragraph. The above amendments to claim 1 obviate the grounds for rejection. Withdrawal of the rejection is respectfully requested.

Applicants gratefully acknowledge the Office Action's indication that claims 3-7 and 9 are allowable over the prior art of record. By this Amendment, new claims 10-15 are added. New claims 10-15 generally correspond to original claims 3-7 and 9 (with original claim 1 slightly modified). Thus, each of claims 10-15 are believed to be allowable over the prior art of record.

The Office Action rejects claims 1 and 8 under 35 U.S.C. § 102(e) by U.S. Patent 6,088,286 to Yamauchi et al. The Office Action also rejects claims 1-2 under 35 U.S.C. § 102(e) by U.S. Patent 6,366,520 to Huber. The rejections are respectfully traversed.

Independent claim 1 recites a node arranged in the vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit are connected through a second long-distance

wiring and a speed-increasing circuit. For example, as discussed in the present application, a second long-distance wiring 106 and a speed-increasing circuit 107 may be arranged in parallel to the driver circuit 100 and a first long-distance wiring 104. The two parallel lines may be connected at the input terminal of the driver circuit 100 and at the node 105 in the vicinity of an input terminal of the gate circuit 103. Accordingly, embodiments may solve a problem that a signal waveform input to a gate circuit at the farthest end from a driver circuit loses sharpness and becomes a round waveform due to wiring delay so that an operational speed of the semiconductor integrated circuit decreases. Thus, in the present application even at the farthest gate circuit from the driver circuit, sharp signal waveform may be obtained in a similar manner as at a gate circuit near the driver circuit.

On the other hand, Yamauchi relates to increasing an operational speed of a memory by dividing a word line into a main word line (MWL) and a sub-word line (SWL). In Yamauchi, the main word line and sub word line are connected at one end. Yamauchi does not teach or suggest that the other ends of the main word line and the sub word line are connected. Accordingly, Yamauchi does not teach or suggest all the features of independent claim 1.

Huber does not teach or suggest a first long-distance wiring as recited in claim 1. The Office Action appears to state that the claimed first long distance wiring corresponds to the wire carrying the output of the driver 110. This may be interpreted in one of two ways. In a first interpretation, the alleged first long-distance wiring may be interpreted as the line between the inverter 110 and the inverter 120.

However, in this case, Huber's structure is very different from the present application. In the second interpretation, the alleged first long-distance wiring may be interpreted as the output of the inverter 110 to a transistor 208 through the inverter 120. However, in this interpretation, Huber's structure is also very different as compared with the present application.

Furthermore, the Office Action asserts that Huber's capacitor 128 presumably corresponds to a furthest gate circuit. However, under the first interpretation discussed above, the furthest gate circuit would be the transistor 182 and under the second interpretation, the furthest gate circuit would be the transistor 208. Accordingly, the Office Action's understanding is incorrect.

Additionally, Huber does not teach or suggest increasing an operational speed of a gate circuit located at the farthest end from the driver circuit so as to obtain a similar sharp signal waveform as at a gate circuit nearest to the driver circuit. The Office Action alleges that Huber's transistor 166 corresponds to the claimed speed-increasing circuit. However, the transistor 166 does not have a function of increasing the operational speed of the farthest gate circuit. See Huber's column 6, lines 19-38. In Huber, the longer the line carrying the output of the inverter 110, the signal waveform input to the farthest gate circuit loses sharpness as compared with the gate circuit nearest the inverter 110. Accordingly, Huber clearly differs from the present application.

Although not discussed in the Office Action, there is no suggestion to combine Yamauchi and Huber. Furthermore, even if combined, the combination of

Yamauchi and Huber does not teach or suggest all the features of independent claim 1. Accordingly, independent claim 1 defines patentable subject matter. Claims 2-9 depend from claim 1 and therefore also define patentable subject matter. Withdrawal of the outstanding rejections is respectfully requested.

Applicants additionally filed an Information Disclosure Sheet (and nine cited references) on August 17, 2001. The Examiner is requested to initial the Information Disclosure Sheet so as to show the consideration of the references.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the above- identified application is in condition for allowance. Favorable consideration and prompt allowance of claims 1-15 are respectfully requested.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the

deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (500.40501X00).

Respectfully submitted,

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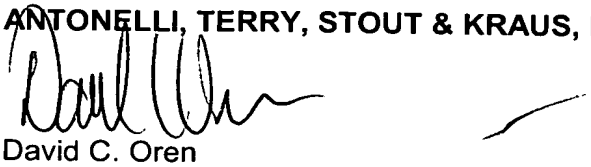

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 6 have been amended as indicated below.

1. (Amended) A semiconductor integrated circuit device comprising a driver circuit, a first long-distance wiring connected to the driver circuit, and a plurality of gate circuits connected over the entire length of the first long-distance wiring, so that an input signal VIN is received by the plurality of gate circuits via the driver circuit and the first long-distance wiring,

wherein a node arranged in the vicinity of an input terminal of the gate circuit connected to an end of the first long-distance wiring and an input terminal of the driver circuit [and an end of the first long-distance wiring is connected by] are connected through a second long-distance wiring and a speed-increasing circuit.

6. (Amended) The semiconductor integrated circuit device as claimed in Claim 1, wherein a plurality of buffer circuits [and] are inserted at the input side of the second long-distance wiring.

New claims 10-15 have been added.